

n re the Application of: HASHIMOTO, Hiroshi et al.

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Group Art Unit: 2814

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Examiner: Howard WEISS

Filed: September 24, 2001

Serial No.: 09/960,399

P.T.O. Confirmation No.: 5652

For. SEMICONDUCTOR INTEGRATED CIRCUIT AND FABRICATION PROCESS

THEREOF

PETITION FOR EXTENSION OF TIME

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Date: May 23, 2005

Sir:

Applicants petition the Commissioner for Patents to extend the time for response to the Office Action dated February 3, 2005 for one month, from May 3, 2005 to June 3, 2005.

Attached please find a check in the amount of \$120.00 to cover the cost of the extension for a large entity. In the event that any additional fees are due in connection with this paper, please charge our Deposit Account No. 01-2340.

Respectfully submitted,

ARMSTRONG, KRATZ, QUINTOS, HANSON & BROOKS, LLP

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Atty. Docket No. **011225**

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